

AMENDMENTS TO THE CLAIMS

This is a complete and current listing of the claims, marked with status identifiers in parentheses. The following listing of claims will replace all prior versions and listings of claims in the application.

Claims 1-6 (**Canceled**).

7. **(Currently Amended)** ~~The input buffer circuit of claim 5, wherein the current controlling circuit comprises:~~ An input buffer circuit comprising:
 a first inverting switch connected to a first input voltage and outputting a self bias signal;
 a second inverting switch connected to a second input voltage and outputting an output signal;
 a gain control unit having a dual feedback loop for gain control responsive to the self bias signal and the output signal; and
 a current controlling circuit that supplies current to the first inverting switch, the second inverting switch and the gain control unit and sinks current from the first inverting switch, the second inverting switch and the gain control unit, the current controlling circuit responding to the self bias signal; and
 wherein
 the gain control unit includes,

a first PMOS transistor having a source connected to a first node, a drain connected to the self bias signal and a gate connected to the output signal;

a first NMOS transistor having a source connected to a second node, a drain connected to the self bias signal and a gate connected to the output signal;

a second PMOS transistor having a source connected to the first node, a drain connected to the output signal and a gate connected to the self bias signal;

a second NMOS transistor having a source connected to the second node, a drain connected to the output signal and a gate connected to the self bias signal;

a third PMOS transistor having a source connected to the first node, a drain connected to the gain control unit to supply current and a gate connected to the self bias signal; and

a third NMOS transistor having a source connected to the second node, a drain connected to the gain control unit to sink current and a gate connected to the self bias signal.

Claim 8 **(Canceled)**.

9. **(Currently Amended)** The input buffer circuit of claim [[8]] 11, wherein the gain control unit comprises:

a first PMOS transistor having a source connected to a first node, a drain connected to the self bias signal and a gate connected to the output signal;

a first NMOS transistor having a source connected to a second node, a drain connected to the self bias signal and a gate connected to the output signal;

a second PMOS transistor having a source connected to the first node, a drain connected to the output signal and a gate connected to the self bias signal; and

a second NMOS transistor having a source connected to the second node, a drain connected to the output signal and a gate connected to the self bias signal.

10. **(Original)** The input buffer circuit of claim 9, wherein the gain control unit further comprises:

a third PMOS transistor having a source connected to the first node, a gate and a drain connected to the self bias signal;

a third NMOS transistor having a source connected to the second node, a gate and a drain connected to the self bias signal.

11. **(Currently Amended)** ~~The input buffer of claim 8, wherein the swing width control circuit comprises:~~ An input buffer circuit comprising:

a first inverting switch connected to a first input voltage and outputting a self bias signal;

_____ a second inverting switch connected to a second input voltage and
outputting an output signal;

_____ a gain control unit having a dual feedback loop for gain control
responsive to the self bias signal and the output signal; and

_____ a swing width control circuit connected to a feedback signal that is
inverted by the output signal, the swing with control circuit including,

an NMOS transistor having a source connected to the gain control
unit, a drain connected to the gain control unit and a gate connected to
the feedback signal; and

a PMOS transistor having a source connected to the output signal,
a drain connected to the gain control unit and a gate connected to the
feedback signal.

Claims 12-24 **(Canceled)**.